JOHNS HOPKINS
APPLIED PHYSICS LABORATORY

LSIC Surface Power Telecon

April 13th, 2023

Begins at 11:03

Lunar Surface Innovation
CONSORTIUM

Dr. Matt Clement, Dr. James Mastandrea, Dr. Sean Young,
Sam Andrade, Julie Peck, Dr. Joseph Kozak, Claire Trop
Johns Hopkins Applied Physics Laboratory
Space Exploration Sector

LSIC Surface Power Facilitator POC: matt.clement@jhuapl.edu

LSIC | Agenda

- Community Updates
  - Solicitations and Awards
  - Conferences/Workshops
    - LSIC Spring Meeting
    - May Telecon: VSAT Phase II
    - July 26-27: LSIC Surface Power Reliability Workshop

- LuSTR Program Overview (Julie Peck)

- LuSTR 2020 Power Awardee Presentations
  - Art Witulski (Vanderbilt)
  - Philip Lubin (UCSB)
  - Jin Wang (OSU)

- Q&A

LSIC | Solicitations and Awards

Space Tech Solicitations (https://www.nasa.gov/directorates/spacetech/solicitations)

LuSTR 2023 Opportunities
Full proposals due April 24

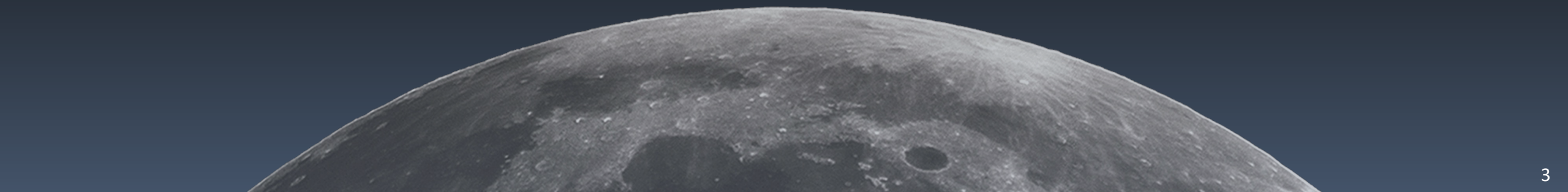
NASA Innovative Advanced Concepts (NIAC) Phase III Call for Proposals
Final Proposals Due: May 17

Early Career Faculty STMD Research Grants
Proposals Due **TODAY**

Early Stage Innovation Solicitation
Solicitation release planned in April 2023

SmallSat Technology Partnerships
Solicitation release coming soon!

TechFlights Solicitation
Solicitation release coming soon!



LSIC | Upcoming Meetings and Workshops

Space Resources Week 2023
April 19-21, Luxembourg

LSIC Spring Meeting
April 24-25, Laurel, MD

LSIC Workshop: Space Technology Competitive Opportunities
April 26, Laurel, MD

Nuclear and Emerging Technologies for Space (NETS 2023)
May 7-11, Idaho Falls, ID

Space Resources Roundtable (SRR)
June 2-5, Golden, CO

More complete calendar on LSIC website, email with additional events!

Lunar Surface Innovation Consortium

ONSITE AT JOHNS HOPKINS APL & ONLINE VIA ZOOMGOV

SPRING MEETING 2023 • APRIL 24–25

REGISTER NOW

DEADLINES TO REGISTER:
APRIL 10 (ONSITE) I APRIL 17 (VIRTUAL)

Scan for more info

FEATURED SPEAKERS

- Pam Melroy, Deputy Administrator, NASA
- Stefanie Tompkins, Director, DARPA
- Matt Daniels, Assistant Director for Space Security and Special Projects, White House OSTP
- Kurt "Spuds" Vogel, Director of Space Architecture, NASA
- James Reuter, Associate Administrator, NASA STMD
- Walt Engelund, Deputy Associate Administrator for Programs, NASA STMD

APL JOHNS HOPKINS
APPLIED PHYSICS LABORATORY

LSIC | May Telecon

We hope to see you all at our next telecon, which will take place on **Thursday May 25th, 2023 at 11:00AM ET.**

Theme: NASA VSAT Phase 2

Speakers:

- **Chuck Taylor**

VSAT PM, NASA

- **Ryan Wiseman**

VSAT Business Lead, Lockheed Martin

- **Dean Bergman**

VSAT PI, Honeybee Robotics

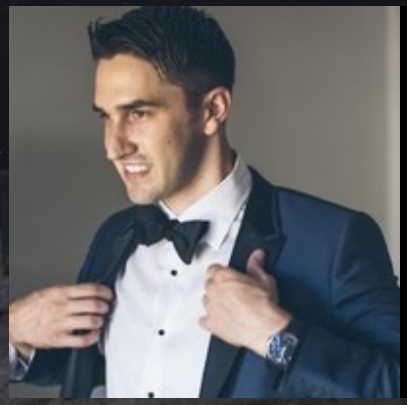
- **John Landreneau**

VSAT PM, Astrobotic

Chuck Taylor

Ryan Wiseman

Dean Bergman



John Landreneau

LSIC | Surface Power Reliability Workshop

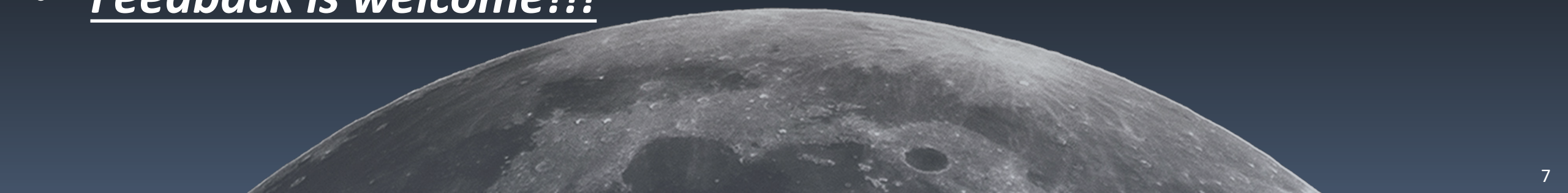
- July 26-27
  - 11:00AM – 3:30 PM ET

- What is Reliability?
  - Redundancy? Resiliency? Interoperability? Maintenance-free?

- How do we approach reliability from the system/grid level and how should this affect the early-TRL development at the component level?

- Bring in Different Perspectives
  - ESDMD, STMD, Industry, Terrestrial Grids, Microgrids, DoD, USN SUBSAFE, and you!

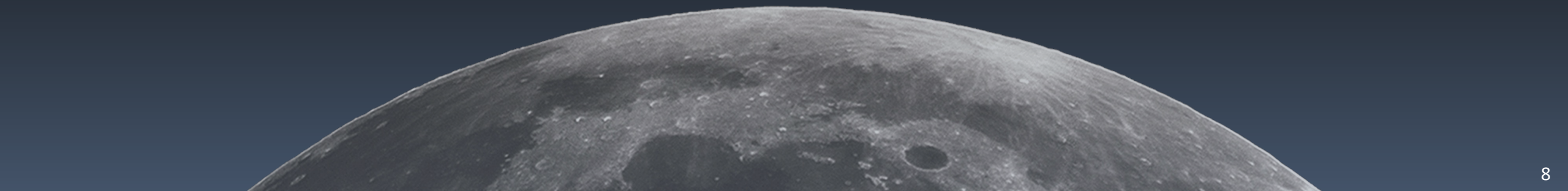
- ***Feedback is welcome!!!***



LSIC | LuSTR Program Overview

LuSTR – Lunar Surface Technology Research

- Part of NASA's Space Technology Research Grants (STRG) program and the Lunar Surface Innovation Initiative (LSII)
  - The LuSTR program seeks proposals that are responsive to specific LSII focus areas
- Grants are awarded to teams from accredited U.S. universities
  - Maximum of two years
  - Maximum award of $2 million to selected teams
- The goal of the LuSTR program is to advance technologies for lunar surface exploration and accelerate the technology readiness of key systems
  - Technologies developed under LuSTR will directly support the Artemis program



LSIC | LuSTR Awards

Year	Recipient	Topic	LSII Focus Area
2020	**Arthur Witulski** *Vanderbilt University*	Silicon Carbide Power Components for NASA Lunar Surface Applications	Sustainable Power
	Philip Lubin *University of California, Santa Barbara*	Moonbeam-Beamed Lunar Power	Sustainable Power
	Jin Wang *Ohio State University*	Flexible DC Energy Router based on Energy Storage Integrated Circuit Breaker	Sustainable Power
	Ahsan Choudhuri *University of Texas, El Paso*	Advanced Thermal Mining Approach for Extraction, Transportation, and Condensation of Lunar Ice	In Situ Resource Utilization
	Paul van Susante *Michigan Technological University*	Percussive Hot Cone Penetrometer (PHCP) and Ground Penetrating Radar (GPR) for Geotechnical and Volatiles Mapping	In Situ Resource Utilization
	Alian Wang *Washington University in Saint Louis*	WRANGL3R - Water Regolith ANalysis for Grounded Lunar 3d Reconnaissance	In Situ Resource Utilization
2021	**Christopher Dreyer** *Colorado School Of Mines*	(ASPECT) Autonomous Site Preparation: Excavation, Compaction, and Testing	Excavation/Construction
	Daoru Han *Missouri University of Science and Technology*	Regolith Beneficiation System for Production of Lunar Calcium and Aluminum	Excavation/Construction
	Michael Hamilton *Auburn University*	Cold-Tolerant Electronics and Packaging for Lunar Surface Exploration	Extreme Environments

LSIC | Presentation

- Speaker: Professor Art Witulski
- LuSTR Project: "Silicon Carbide Power Components for NASA Lunar Surface Applications"

VANDERBILT
School of Engineering

Presentation for LSIC Surface Power Focus Group

Single-Event Effects in Silicon Carbide High Voltage Power Devices for Lunar Exploration

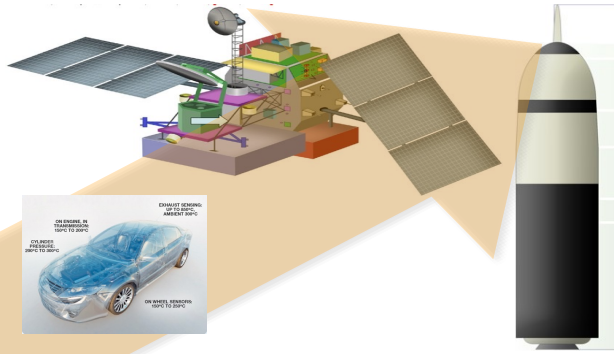
Arthur Witulski
04/13/2023
art.witulski@Vanderbilt.edu
Vanderbilt University

Supported by the NASA LuSTR Program under Grant Number 80NSSC21K0766

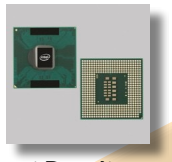
Goal: *Leverage advances in computing power and simulation tools to improve predictive capabilities for robust designs utilizing emerging materials and technologies through the development, validation, and application of multi-scale simulations*

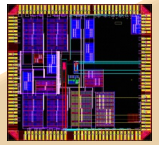
Institute of Space and Defense Electronics (ISDE)
Vanderbilt University

Mission-Critical Systems

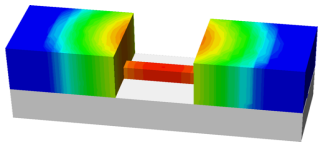


Physical Layout:
Parasitic Models

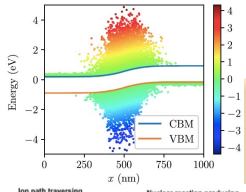




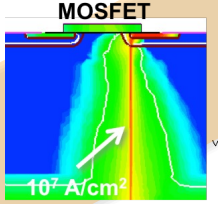
TCAD Device Models



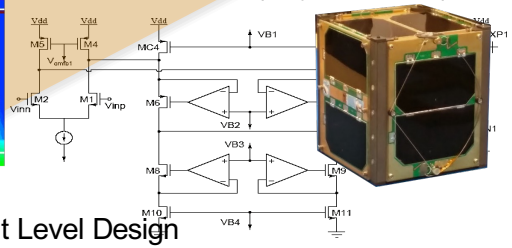
Full-Band Monte Carlo Models



eCurrent Density MOSFET

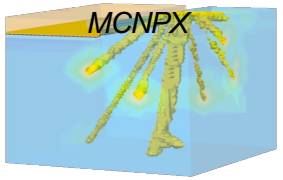


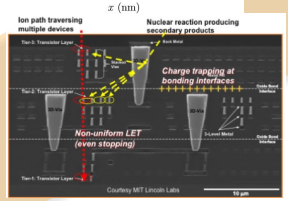
System Analyses
(Bayesian, etc.)



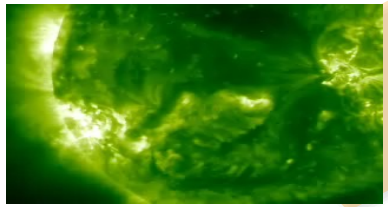
Circuit Level Design
(SPICE, Spectre)

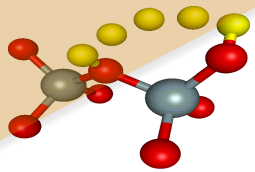
Radiation Transport and Energy Deposition
Geant4 (open source)
MCNPX





Extreme Environment
[Temperature, Radiation, etc.]





Defect Models in structures and at interfaces (DFT, KMC)

Models informed, validated by experimental data

NASA LuSTR SiC Program Call for Proposals

Vanderbilt Engineering

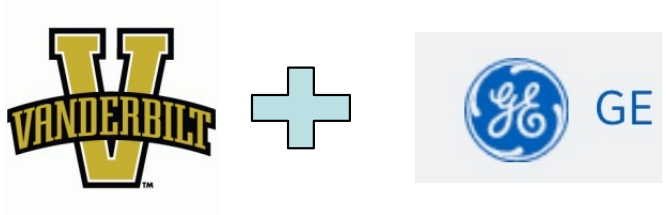
Electrical Performance:

- **SEE-tolerant SiC power diodes: Minimum 1200 V, 40 A, with maximum recovery time of 40 ns**
- **SEE-tolerant SiC power transistors: Normally off (enhancement mode), minimum 600 V, 40 A, Rds_on < 24 mOhms while preserving low switching losses.**

Radiation Goal:

- **No heavy-ion induced permanent destructive effects upon irradiation while in blocking configuration (in powered reverse-bias/off state) with ions having a silicon-equivalent surface incident linear energy transfer (LET) of 40 MeV-cm²/mg of sufficient energy to maintain a rising LET level throughout the epitaxial layer(s).**

- **Application Goal: Micro-Grid on the moon at 1 kV DC**



Power Device Technologies – Why SiC?

Vanderbilt Engineering

ADVANCED POWER TECHNOLOGY®

APT1001RSVR

1000V 11A 1.000Ω

POWER MOS V®

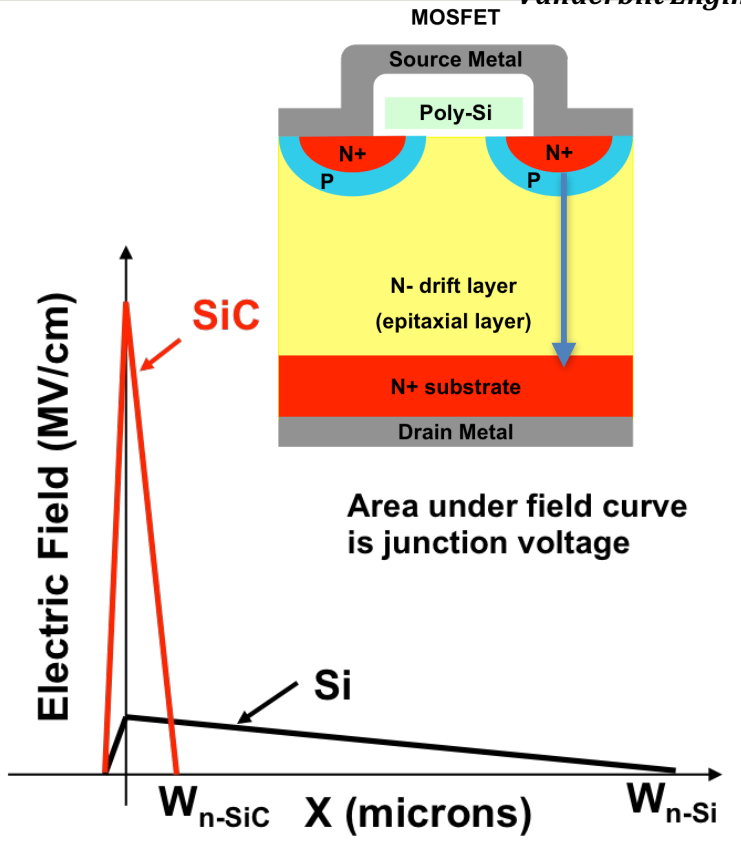
Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V®

CREE

C3M0065100J

Silicon Carbide Power MOS
C3M™ MOSFET Technology
N-Channel Enhancement Mode

V_{DS}	1000 V
$I_{D\ @\ 25^{\circ}C}$	32 A
$R_{DS(on)}$	65 mΩ



On-resistance of SiC ~ 6% of Silicon Device
Much better choice than Si for high voltage

Radiation in Space: Ions, Protons, Electrons

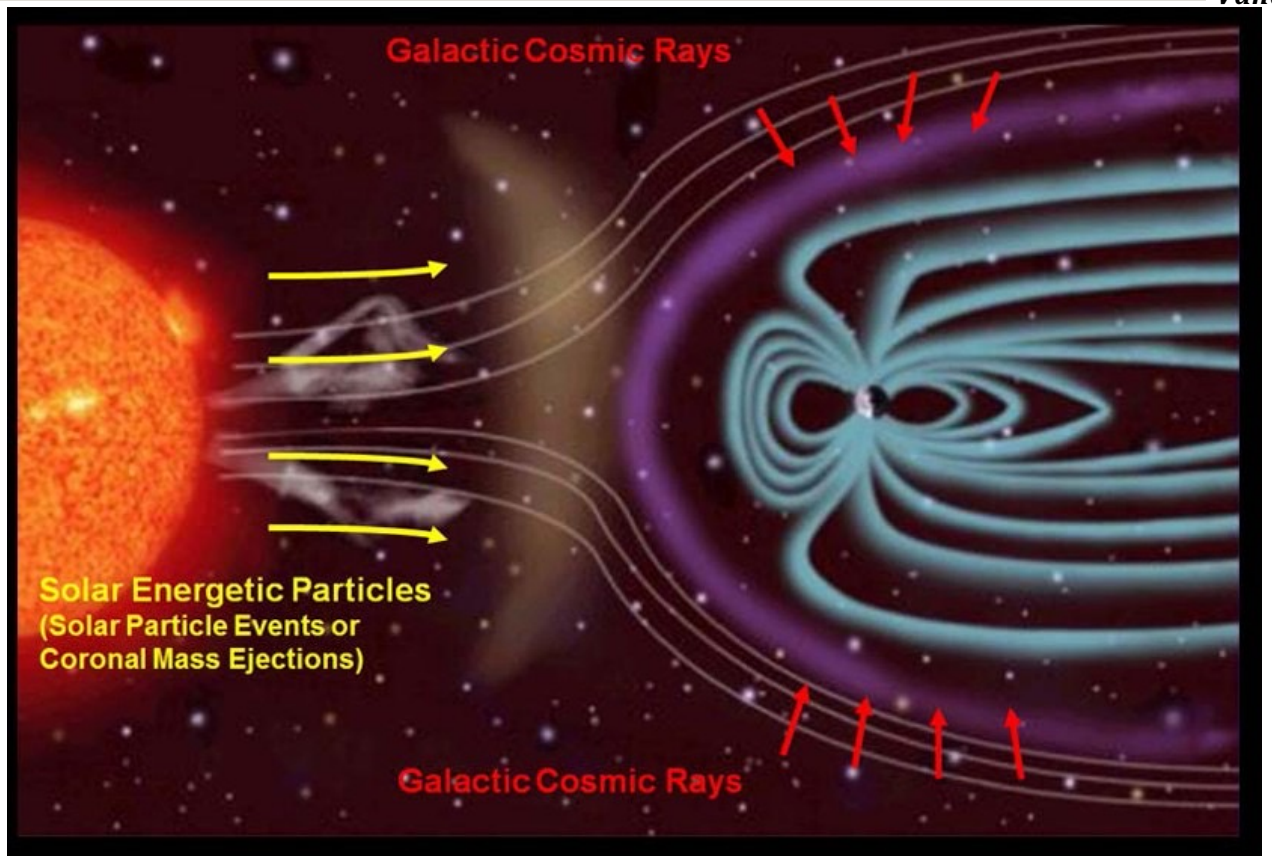
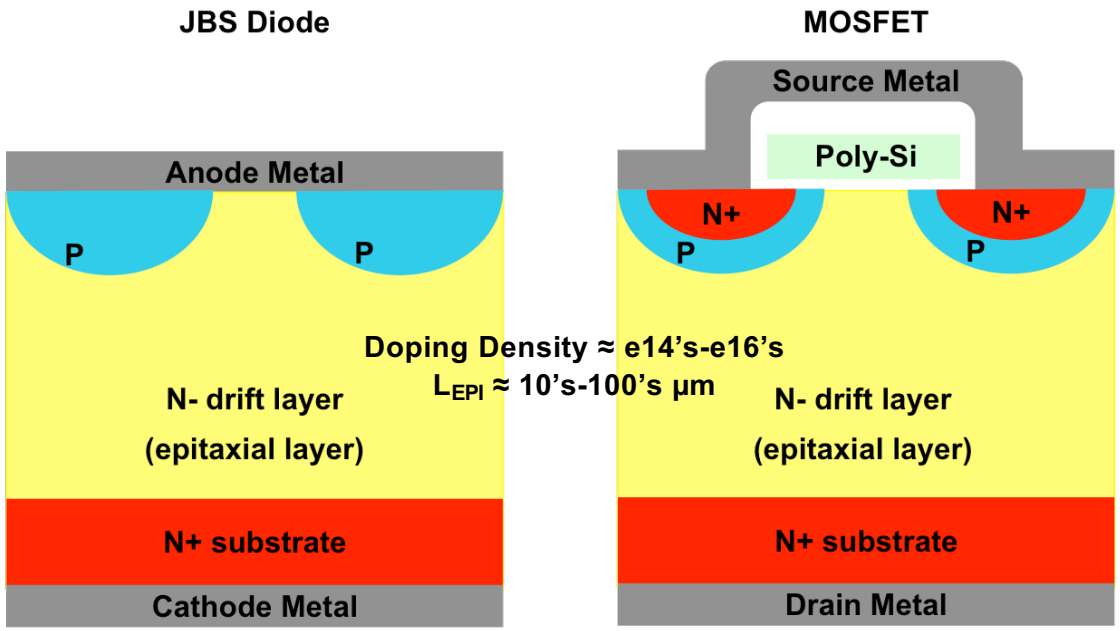


Image credit: NASA/JPL-Caltech/SwRI

Silicon Carbide Vertical Power Devices

Vanderbilt Engineering

- Vertical power device
  - Suitable for diodes and MOSFETs
  - Vertical current flow
  - Performance influenced by epitaxial region resistance

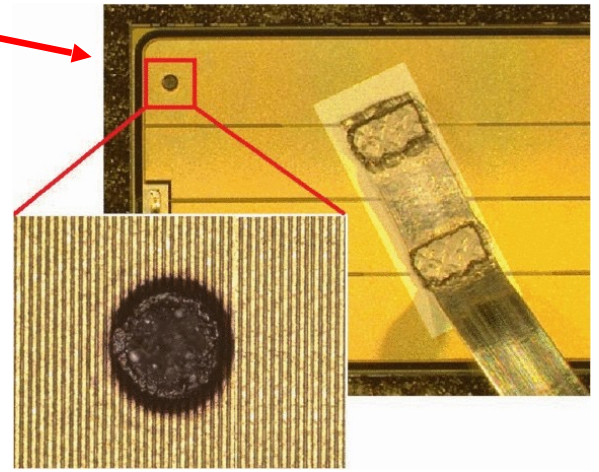


Radiation Effects in Power Devices

Vanderbilt Engineering

- Total Ionizing Dose (TID) – charge trapped in insulating layers
  - Parametric shifts in device electrical characteristics (i.e. threshold voltage)
- Single Event Effects – ions deposit charge in active device regions
  - Transient current/voltage pulses
  - ***Permanent increases in leakage currents***
  - ***Single event burnout (SEB) - catastrophic***

From: G. Consentino et. al, 2014 IEEE Applied Power Electronics Conference and Exposition

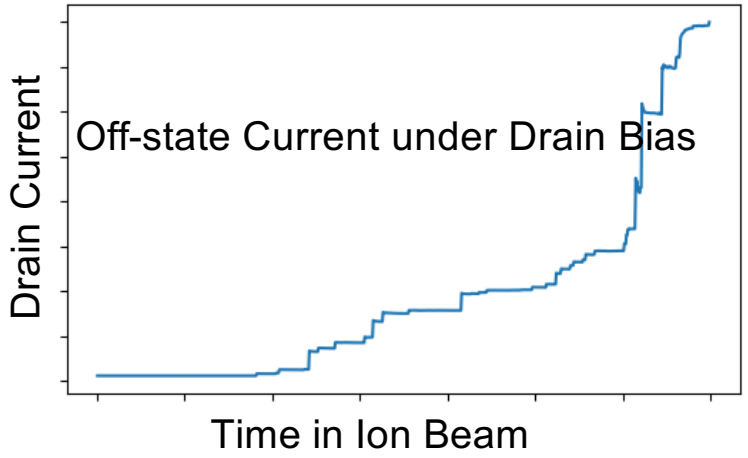


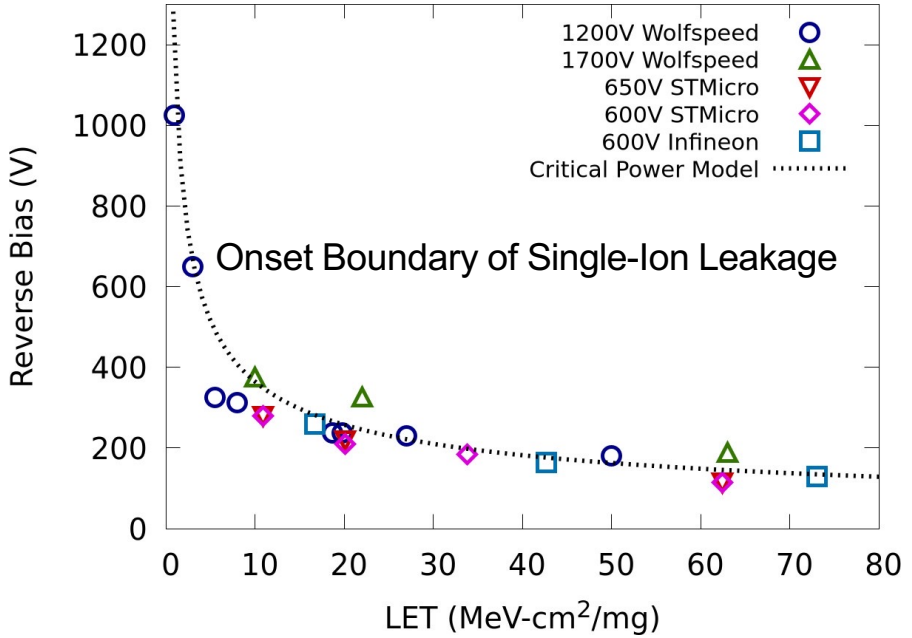
Space applications: Catastrophic failure is not an option!

Single-Event Leakage Current (SELC)

Vanderbilt Engineering

- SiC devices show step changes in off-state current for single ion strikes
- SiC devices show onset of the effect at reverse biases ~20% of rated breakdown voltage.
- Leakage independent of manufacturer or breakdown voltage (epi depth)
- Large enough for parametric failure

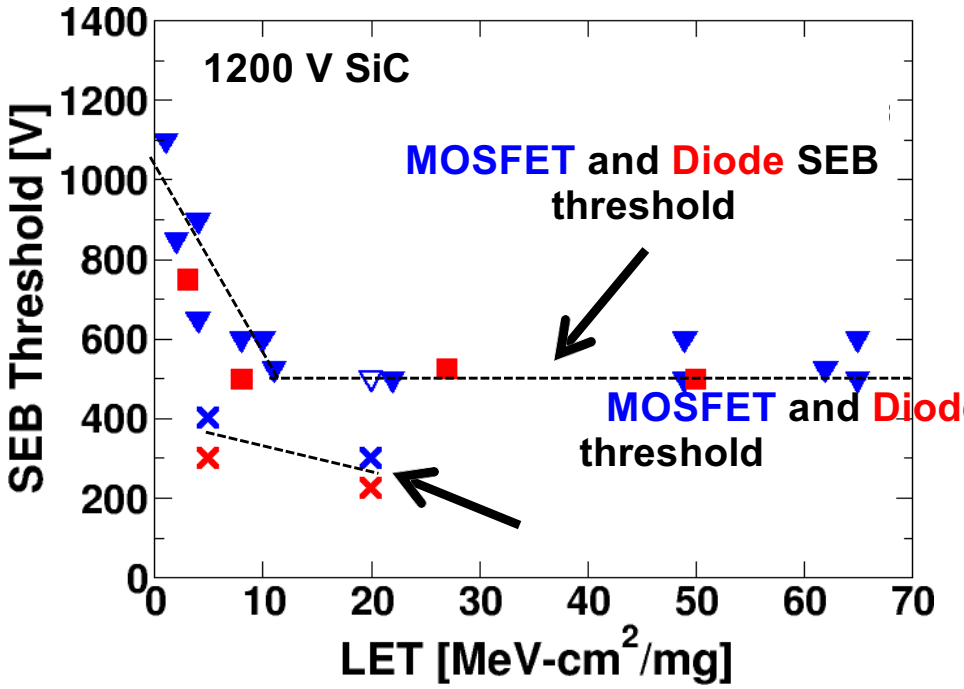




R.A. Johnson, et al, IEEE TNS, Jan. 2020

SEB in 1200 V SiC Vertical DMOS and JBS Schottky

Vanderbilt Engineering



Heavy ion-induced SEB and degradation data for SiC MOSFETs and diodes from:

Mizuta 2014
Lauenstein 2015 (LBNL)
Witulski 2018 (RADEF and TAMU)
"Hockey Stick" curve

- Note that SiC and diodes have the same SEB Bias-LET boundary
- Indicates a similar SEB mechanism

Witulski, et al, IEEE TNS, 2018

Heavy ion data suggests common mechanism(s) responsible for SEB and degradation in SiC

Ion-Induced Current Densities and Re-Distribution of Electric Field

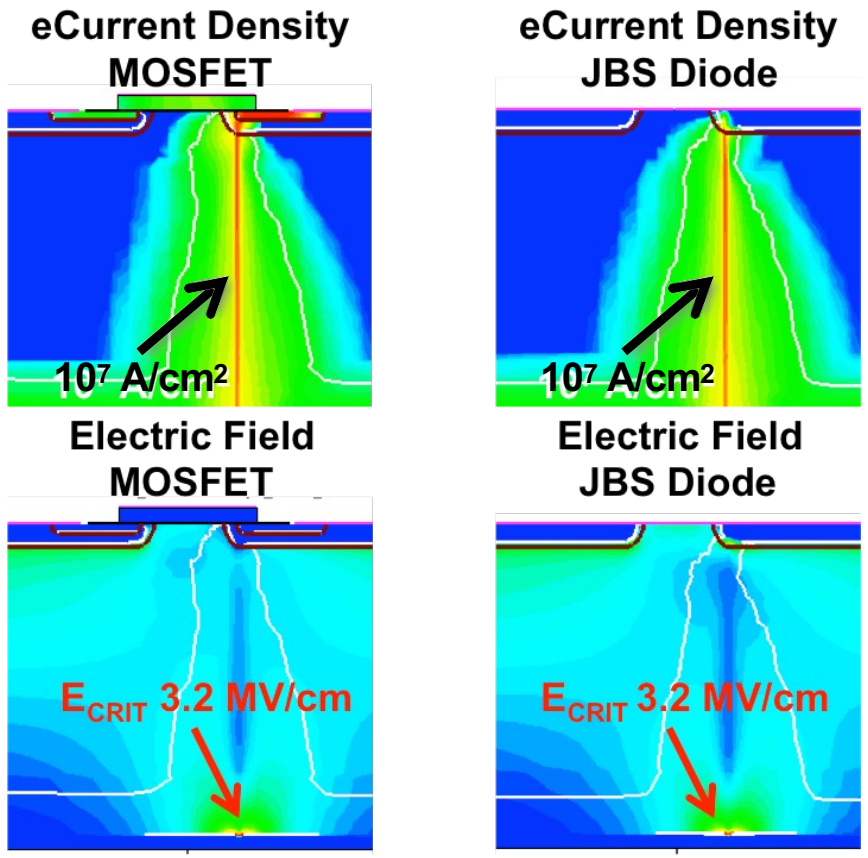
Vanderbilt Engineering

3D TCAD heavy ion simulation of 1200 V SiC

- **LET = 10 MeV-cm²/mg @ 500 V**
- **Short circuit from high carrier density**
- **Re-distribution of electric field**
- **Maximum field goes from 2 to 3.2 MV/cm**

Power density is extremely high along strike path, high current density and high electric field

$$Pd = J \bullet E$$



D.R. Ball et al, IEEE TNS, Vol. 67, 2020

J. McPherson et al, IEEE TNS Vol. 68, 2021

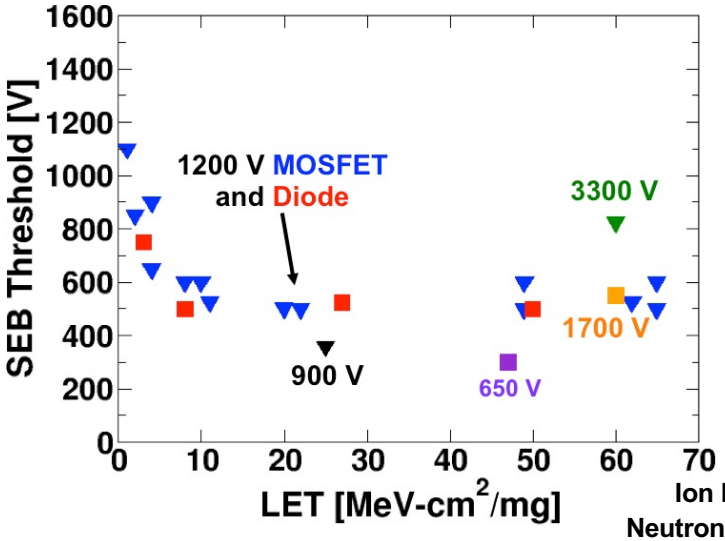
Impact of Voltage Rating on SEB Threshold

Vanderbilt Engineering

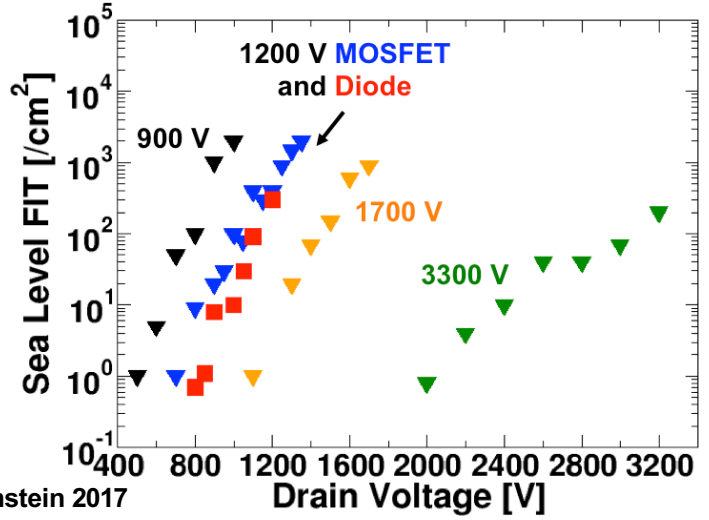
- Ion-induced SEB threshold increases with increasing voltage rating
- Terrestrial neutron-induced SEB FIT rate decreases with increasing voltage rating

Data show increased SEB tolerance for thicker, more lightly-doped epitaxial regions

Ion-Induced SEB



Terrestrial Neutron-Induced SEB

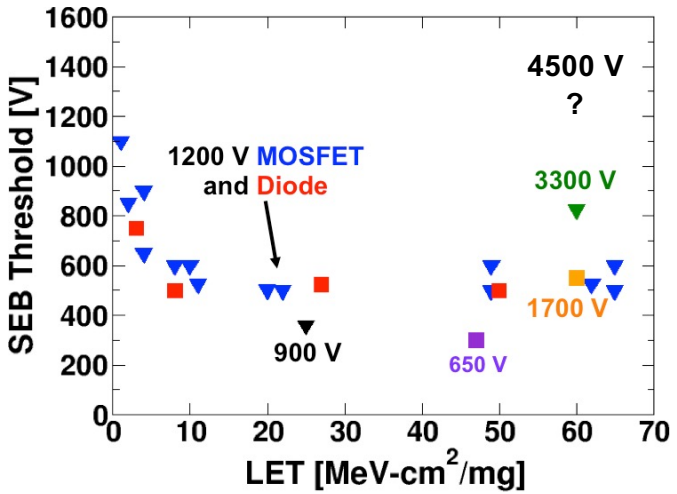


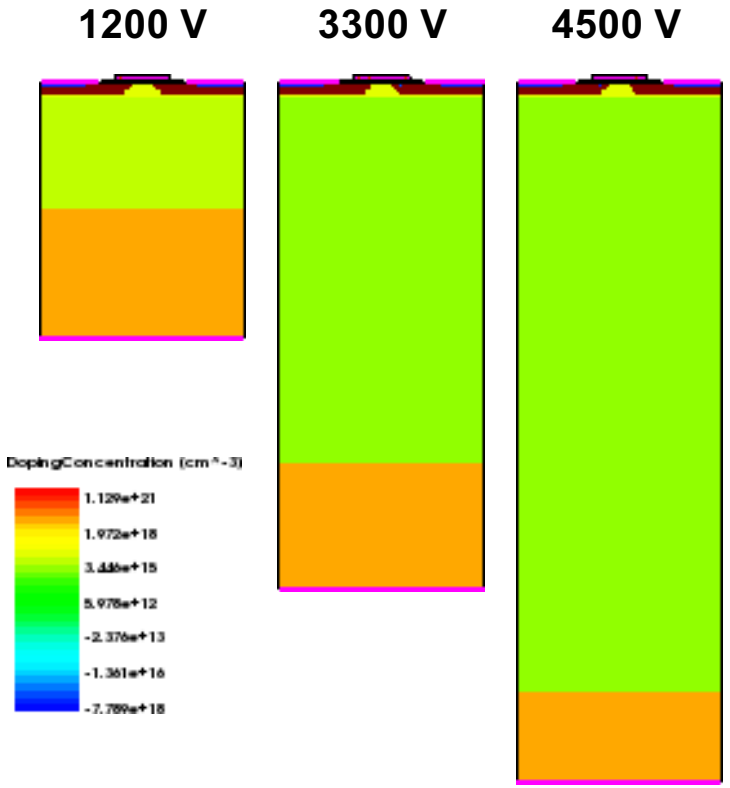
Ion Data from Lauenstein 2017
Neutron Data from Lichtenwalner 2018

Goal: Design Radiation-Tolerant Diode/MOSFET

Vanderbilt Engineering

- VU and GE design device intended to survive catastrophic SEB
- 3D TCAD heavy ion sensitivity study – VU
  - Increase epi thickness
  - Decrease epi doping
  - Effective increase in voltage rating
  - Note: 3300 V device shows SEB @ 850V



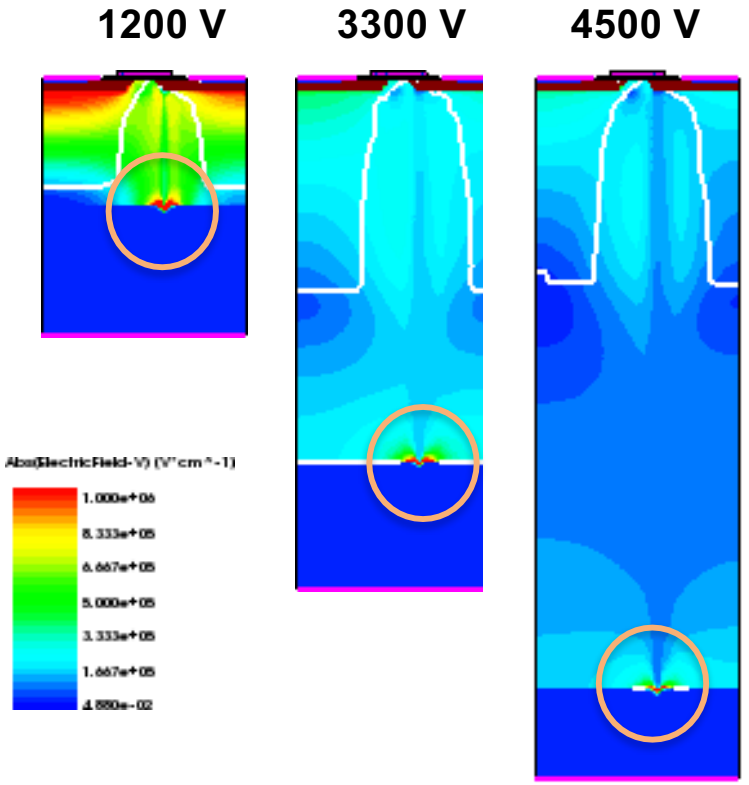


Ion-Induced Electric Field Redistibution

Vanderbilt Engineering

3D TCAD heavy ion simulation of SiC MOSFET variants

- **LET = 60 MeV-cm²/mg @ 500 V**
- **3300 V and 4500 V device show significantly lower electric fields compared to the 1200 V device**



Technical Approach Plan for Baseline 3.3 kV Devices

Deliver Standard Devices

#	Device Type		Project Scope
1	Standard planar MOSFET (1.7kV OR 1.2kV)	Test & establish baseline	Radhard design and fabrication
2	Standard Schottky diode 3.3kV	Test & establish baseline	Radhard design and fabrication
3	Charge-balanced diode 3kV	Test & establish baseline	
4	Charge-balanced MOSFET 3kV	Test & establish baseline	

Design & Fabricate RadHard Devices

TECHNICAL INSIGHTS

- Epi region affects SEB and SELC
- Metal-SiC interface may affect leakage
- Try to keep good electrical performance

DESIGN, FAB, TEST, PACKAGE

- Vary epi thickness and doping to lower peak electric fields
- Some devices have metal windows
- ~ 10 variant devices
- Parallel lots: diodes (~4 months) and MOSFETs (~6months)
- Post-fab tests: Vth, $R_{DS(on)}$, Vdss
- Parylene coating of open-can packages

TECHNICAL CHALLENGES

- Material quality issues including defects, impurities ➔ test bare wafers
- Device design that ensure both electrical performance and rad-tolerance

Apply insights on radiation impact on SiC to implement SEE tolerant power devices

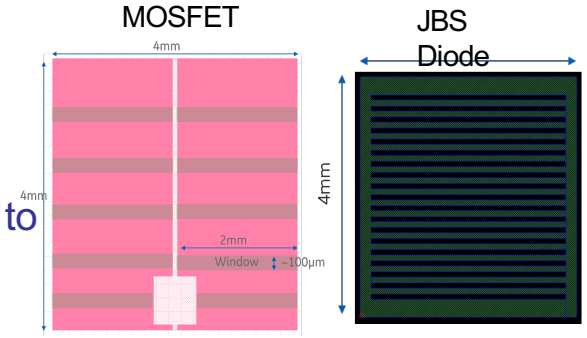
MOSFET and JBS Design

- **Design Strategy**:
  - Design ~4.5 kV device structure. Operate them at 600 V (MOSFETs) or 1200 V (Schottkys) for extra SEE tolerance due to voltage derating

- **Metal Window Splits**:
  - Baseline (No window), 25% opening & 50% opening
  - Designs to be distributed uniformly across the wafer
- **Termination Design***: 4500 V

- **Top JBS Design**: Identify an optimized 4.5kV JBS diode architecture for the lowest surface electric field and lowest Ron.
- **Epi Splits**:
  - Low doping/ Thick epi & High doping / Thick epi

Windows in the active area



Termination design

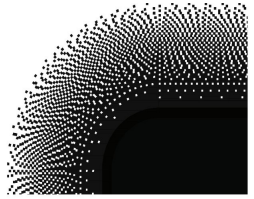
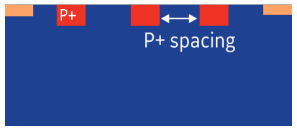


Figure 6. Graded Junction Termination Extension (G-JTE) used to fabricate HV SiC MOSFETs

Top JBS



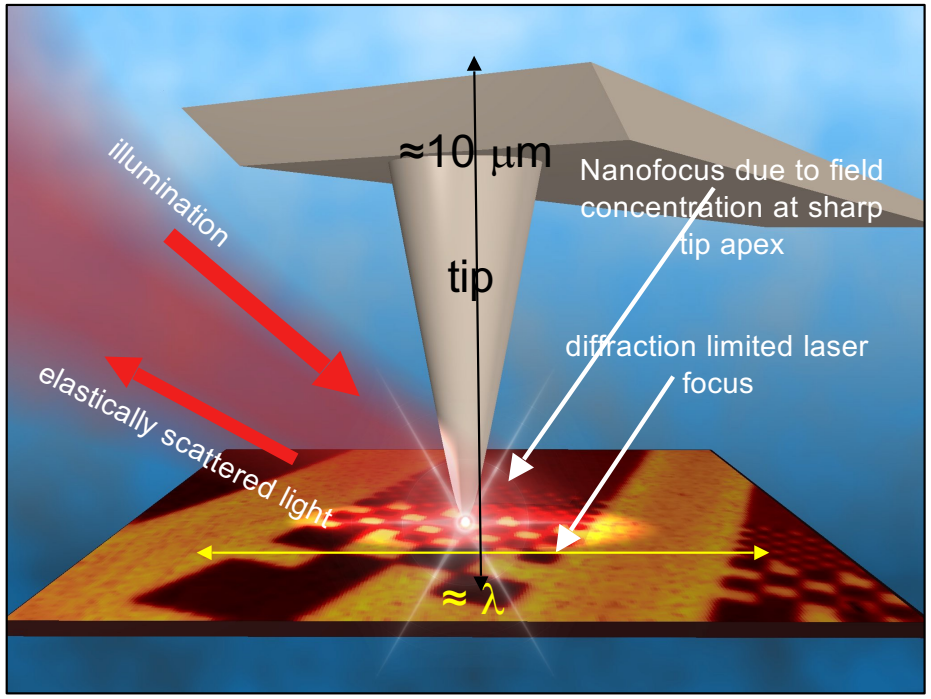
Tradeoff between Ron and surface electric field

*Losee P. A., et al., *SiC MOSFET Design Considerations for Reliable High Voltage*

Achieve SEE resistance by voltage derating of 4.5 kV devices

VU Nanophotonic Materials and Devices Lab

Vanderbilt Engineering



- **Professor Joshua Caldwell**
- **Nano-Optic Probes**
  - Scatter long-wavelength light off of metal AFM tip
  - Use evanescent fields at tip to locally probe optical properties of materials by electroluminescence
- **s-SNOM ➔** spatially map the optical amplitude and phase at one frequency w/ <20-nm spatial resolution!
- **Nano-FTIR ➔** measure FTIR spectra w/ same spatial resolution
- **Pump-probe nano-FTIR ➔** measure FTIR spectra w/ 200 fs temporal resolution following UV (390 nm) or NIR (1560 nm) 130-fs pulse

Summary: Remaining Program Timeline

Vanderbilt Engineering

June 2022 Test GE Baseline 3.3 kV devices at TAMU Ion Accelerator June 2022
Results: 3.3 kV SEB threshold ~300 V higher than 1.2 kV SiC devices
July 2022 New JBS diodes and MOSFETs launched on GE Fab lines
Dec 2022 JBS Diodes exit Fab
Jan. 2023 Electrical testing of diodes
Mar. 2023 Open-cavity TO 257 packaging/Parylene coating
Apr. 2023 Delivery of JBS diodes to Vanderbilt
June 2023 Heavy Ion test of diodes at TAMU
June 2023 SiC MOSFETs exit FAB
July 2023 Electrical Testing
Aug. 2023 Packaging/Parylene
Sep. 2023 Heavy ion test of MOSFETs at TAMU
Dec. 2023 Final Results presented at LSIC Fall Workshop

- Speaker: Professor Philip Lubin
- LuSTR Project: ”Moonbeam-Beamed Lunar Power"

- Speaker: Professor Jin Wang
- LuSTR Project: "Flexible DC Energy Router based on Energy Storage Integrated Circuit Breaker"

Flexible DC-Energy Router based on Energy Storage & Integrated Circuit Breaker

Dr. Jin Wang

Professor, IEEE Fellow

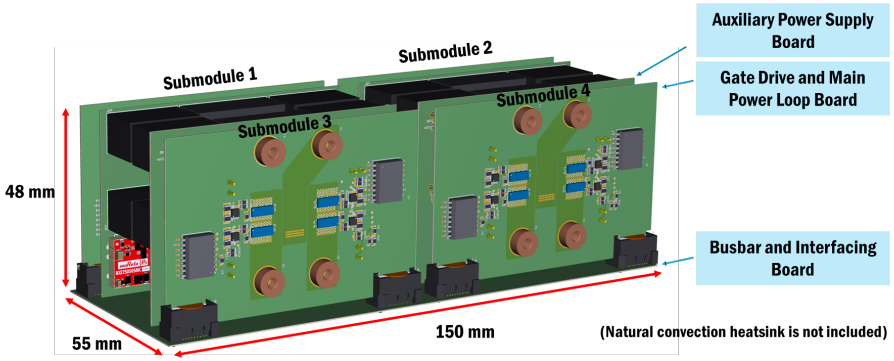
April 13th 2023

The Ohio State University CHPPE | Raytheon Technologies | The Ohio State University Center for Automotive Research

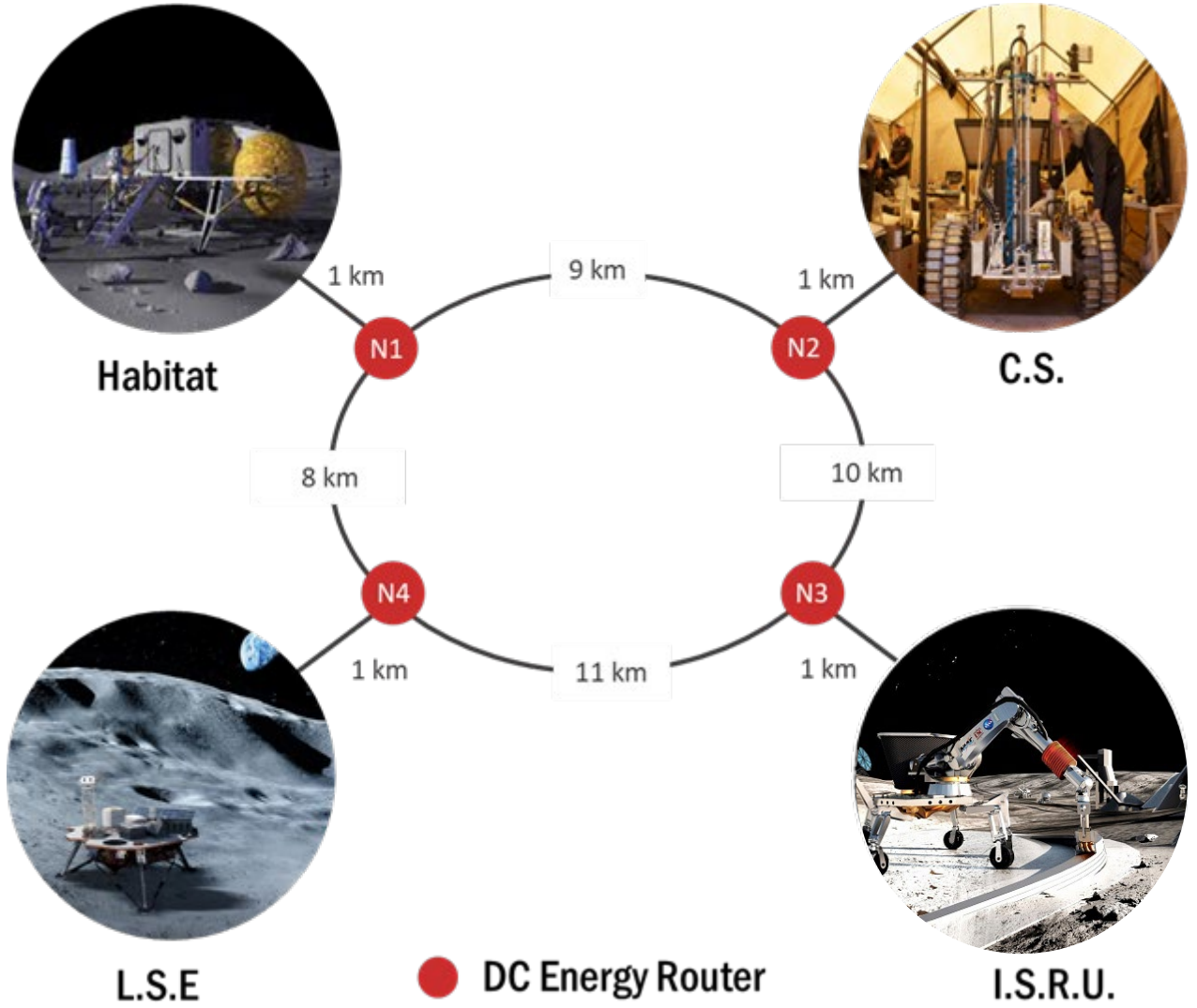
NASA LuSTR: Lunar DC Microgrid with Dc Energy Router

Lunar microgrids interconnected in a ring architecture with DC Energy Routers

Microgrid	Rating
MG1: Habitat	20 kW
MG2: Charging Stations (C.S.)	2 kW
MG3: In-Situ Resource Utilization (ISRU)	60 kW
MG4: Lunar Science Experiments (L.S.E.)	5 kW



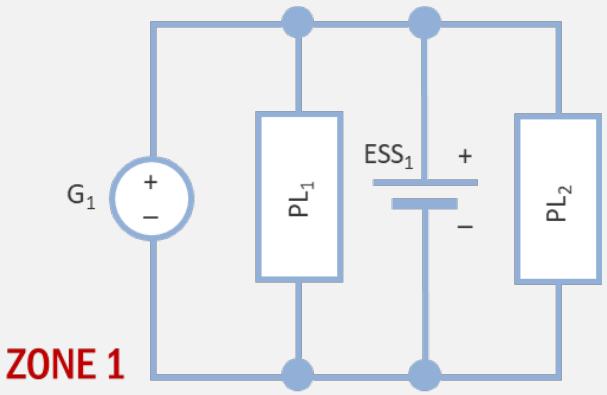
Modular DC Energy Router



Lunar DC Microgrids Model

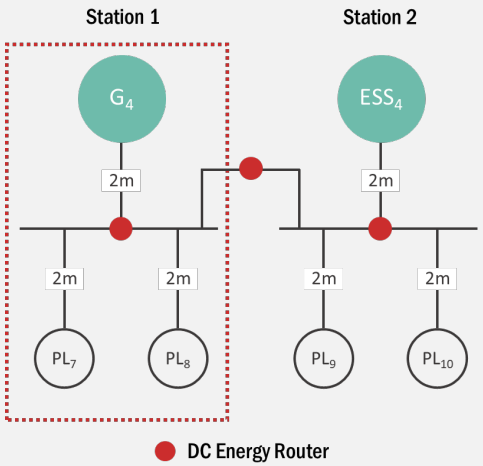
Microgrid I

Habitat



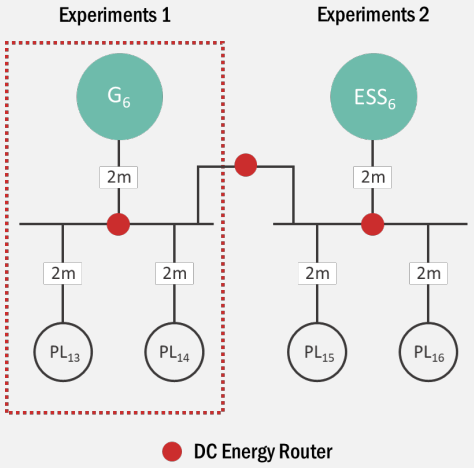
Microgrid II

C.S.



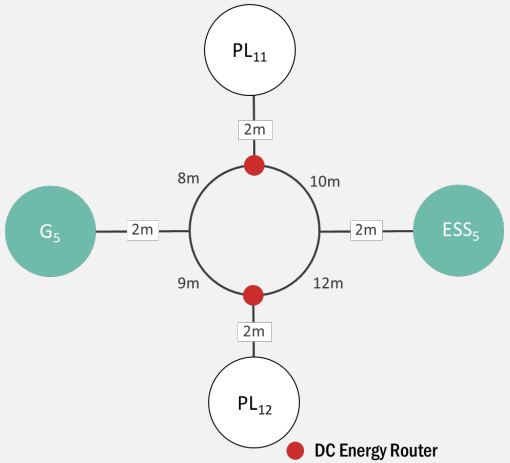
Microgrid IV

L.S.E

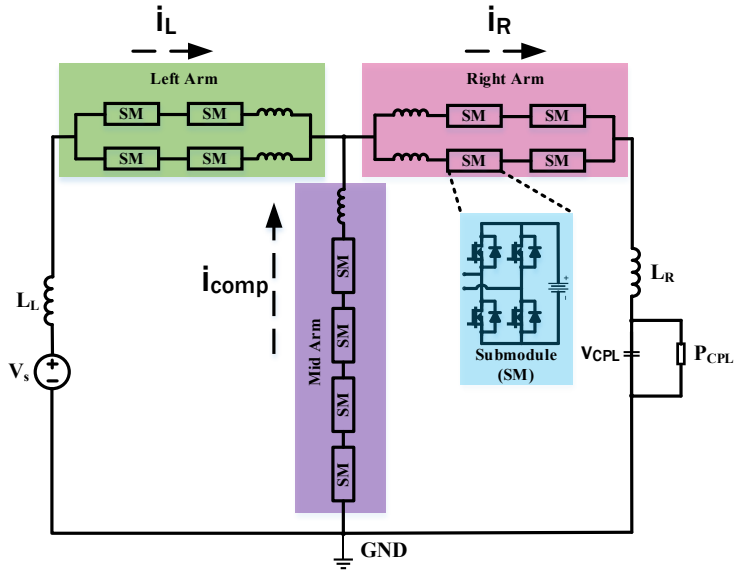


Microgrid III

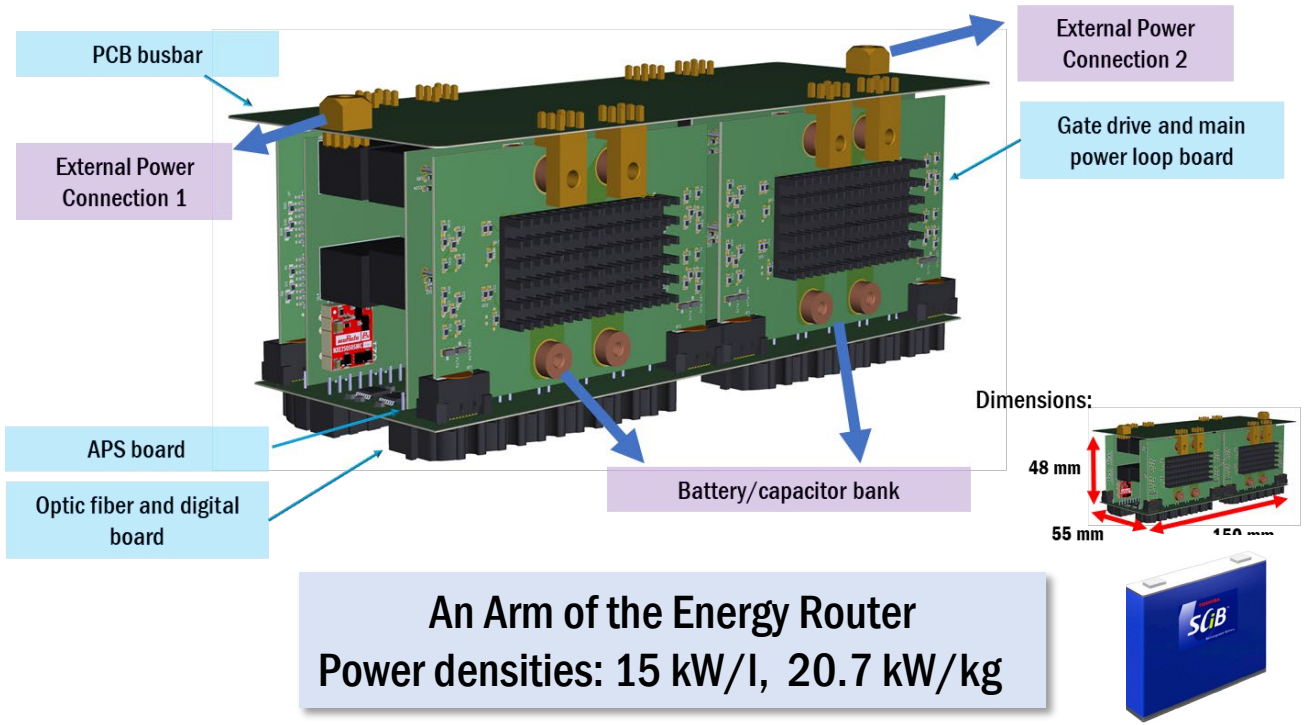
I.S.R.U.



DC-Energy Router



Generic Circuit Diagram of the Proposed DC-Energy Router

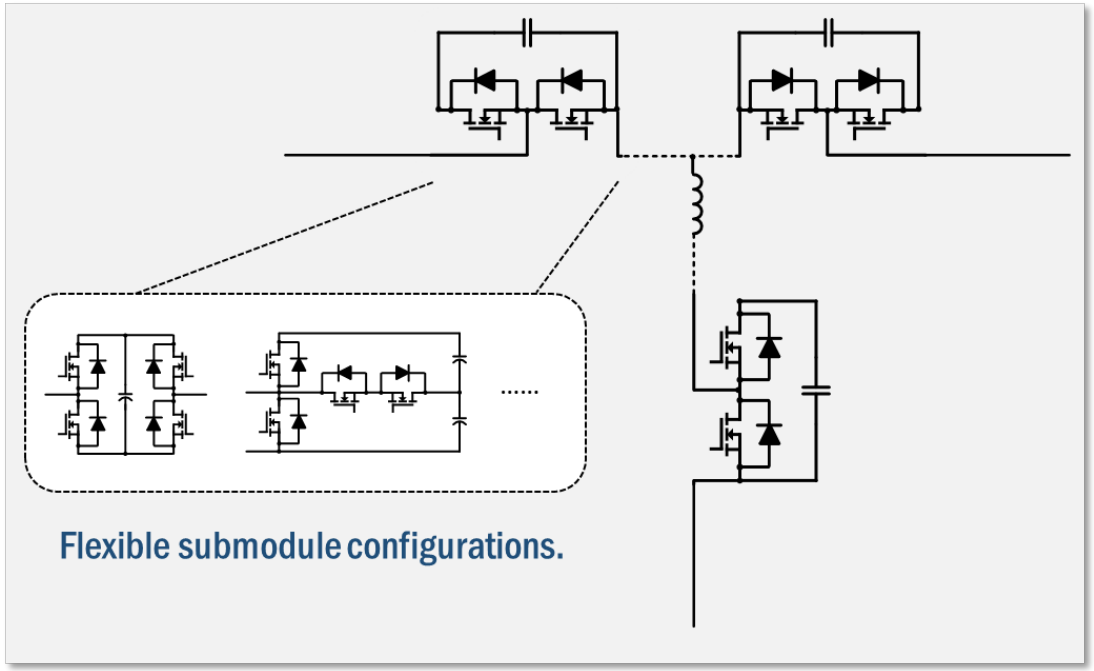


An Arm of the Energy Router
Power densities: 15 kW/l, 20.7 kW/kg

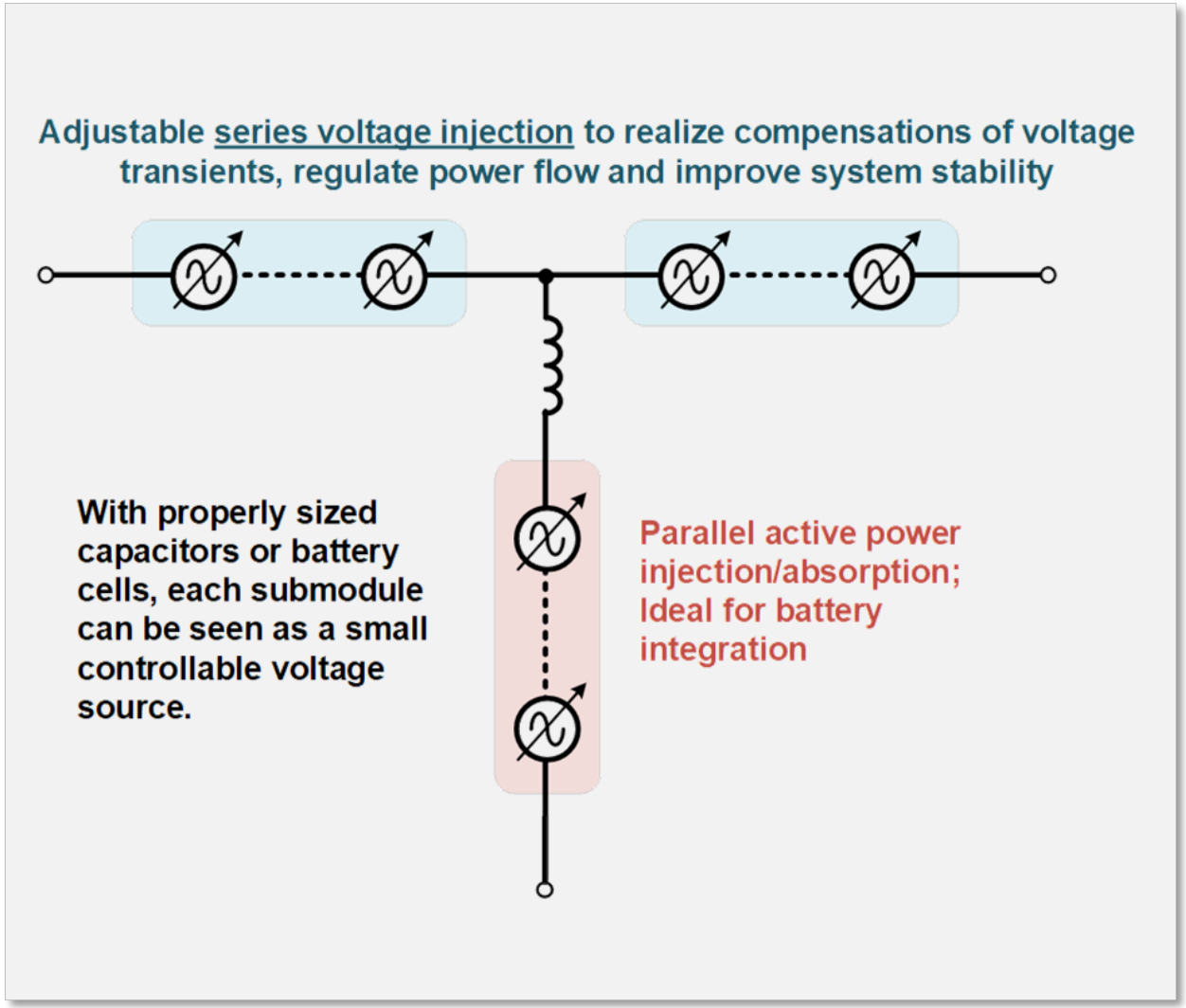
GaN HEMT and Lithium-titanium-oxide (LTO) Battery based Dc Energy Routers

- realize and regulate power flow
- respond to unexpected load and source power changes
- enhance system stability at voltage and power transients

Flexible Submodule Topology Options and Operation Modes



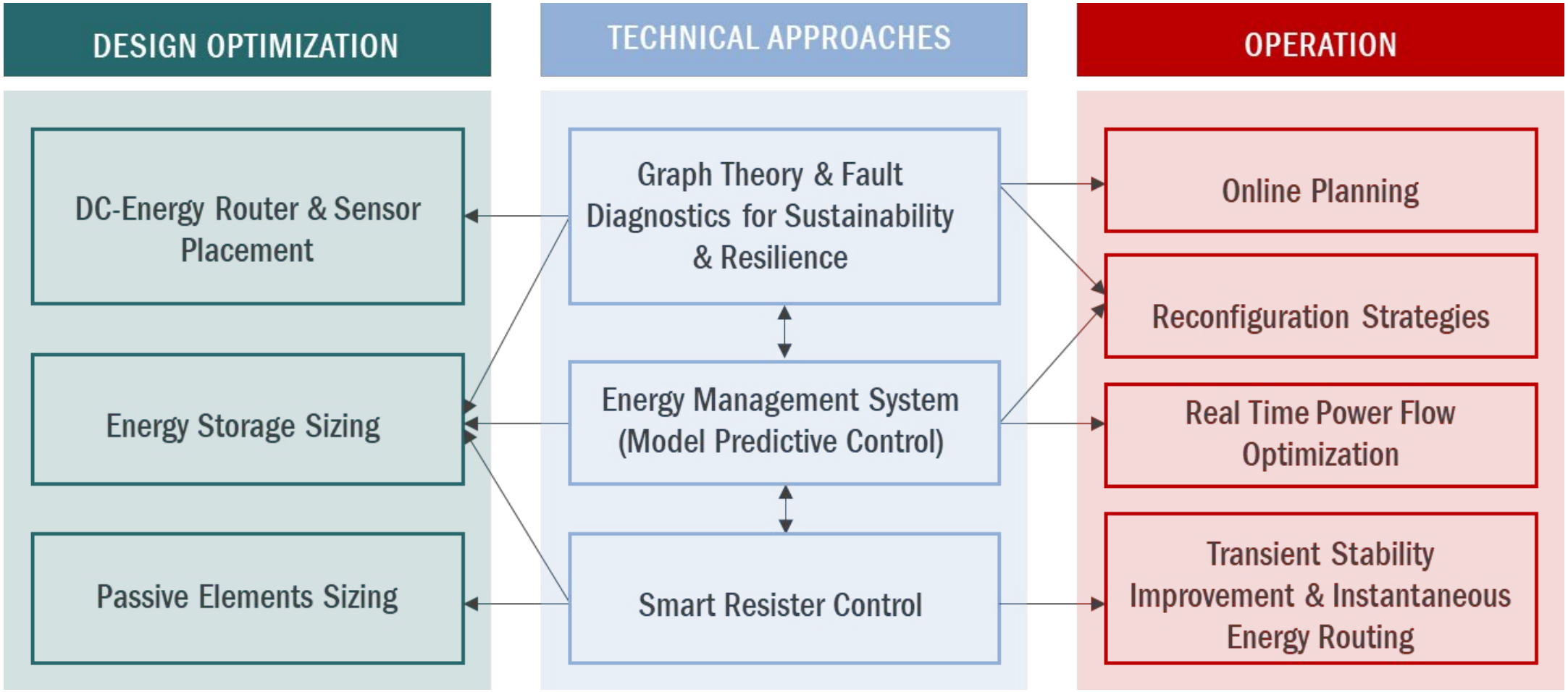
Flexible submodule configurations.



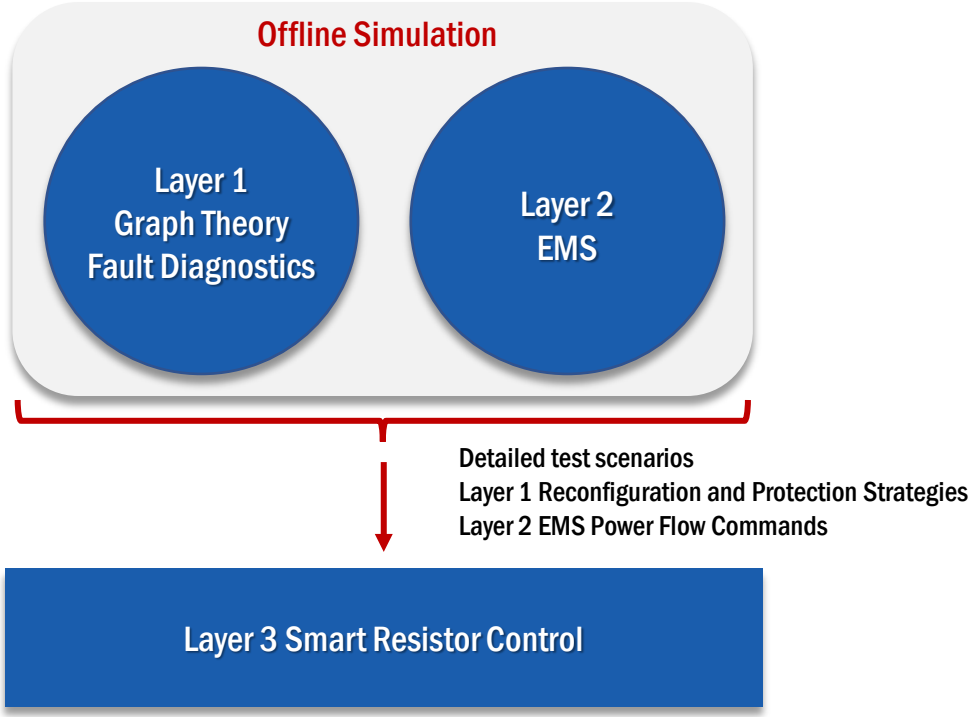
Operation Modes:

- Conduction and fault current breaking as a semiconductor based (solid-state) circuit breaker
- Energy routing by regulating the connection point voltage with series voltage injection
- Power quality and stability improvement

Three-layered Approach

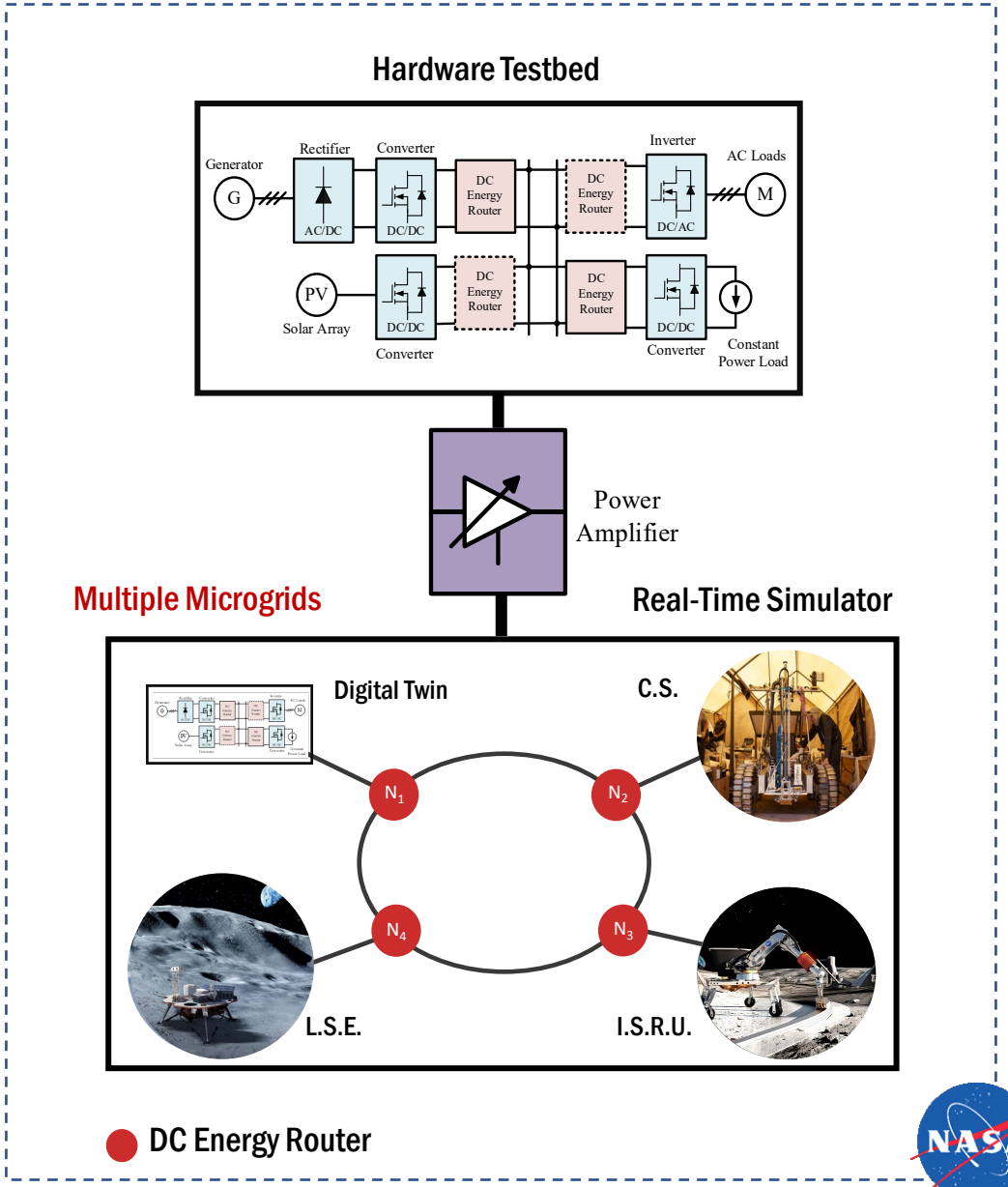


NASA LuSTR Final Demonstration



Power Hardware-in-the-loop testbed to evaluate Layer 3 Control for test cases defined by Layer 1 and Layer 2 studies:

- Normal operation with load and voltage transients
- Fault case 1
- Fault case 2

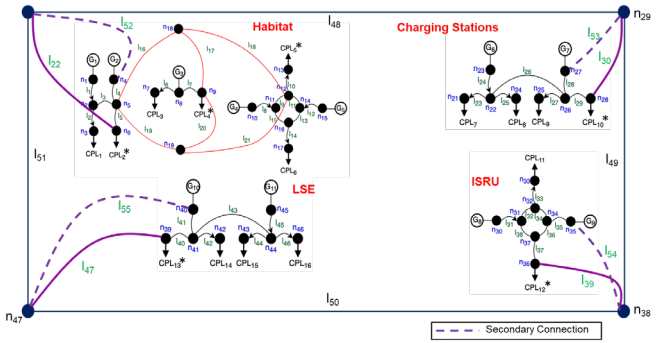


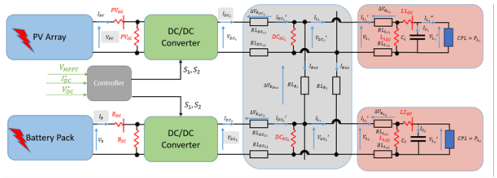
Layer 1 Accomplishments and Ongoing Work

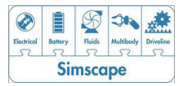
Layer 1: Graph theory-based architecture study; Fault diagnosis; Reconfiguration strategies

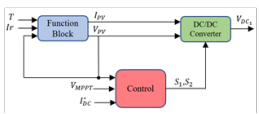
Accomplishments

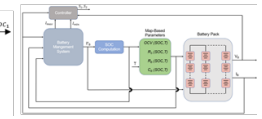
- Hybrid-edge rewiring algorithm to optimize the system architecture for maximized resilience
- N-2 contingency analysis and reconfiguration strategies to minimize load shedding
- Identification of the minimum voltage for inter-connected dc mircrogrids
- System modeling for fault diagnosis
- Optimized sensor placements
- Machine learning based fault diagnosis algorithm











Ongoing and Planned Work

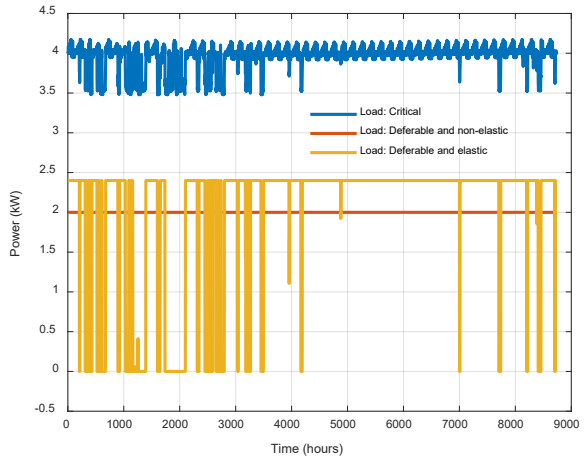
- Finalizing case scenarios for testing and final demonstrations

Layer 2 Accomplishments and Ongoing Work

Layer 2: Energy Management Systems

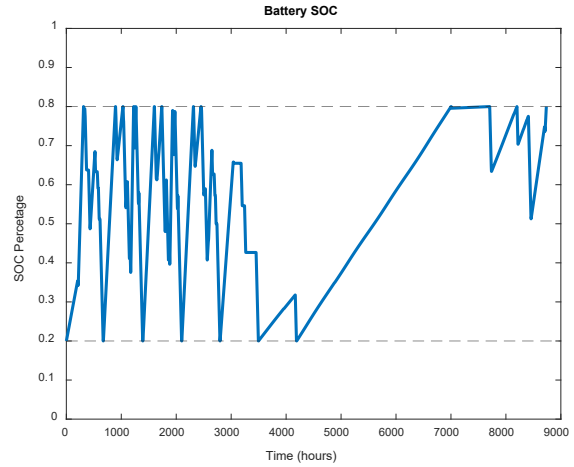
Accomplishments

- Developed EMS algorithm for each microgrid with two-stage optimization:
  - ✓ optimal load scheduling, 1-year time window, updates every 1 hour;
  - ✓ optimal real-time setpoints, 1-week time window, updates every 15 min.



Ongoing and Planned Work

- Further sizing optimization of energy sources and energy storage devices
- Finalizing case scenarios for testing and final demonstrations

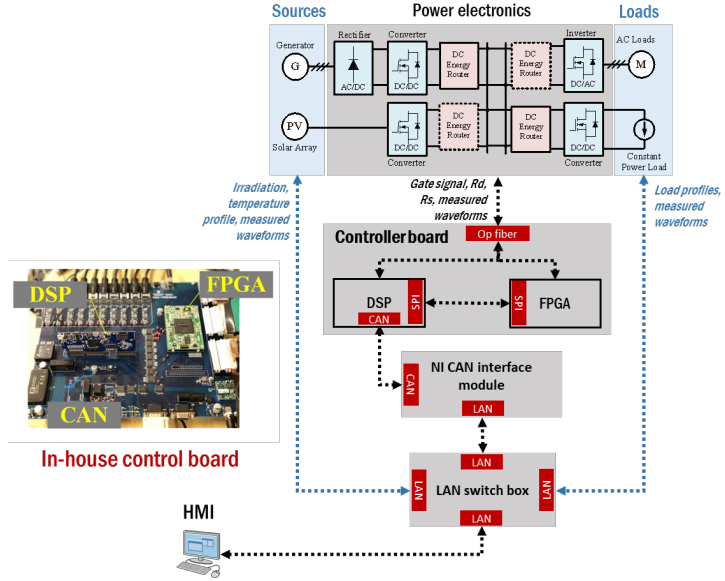


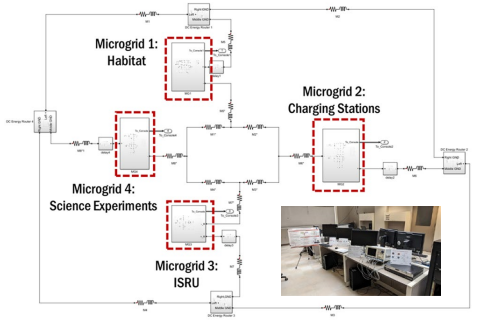
Layer 3 Accomplishments and Ongoing Work

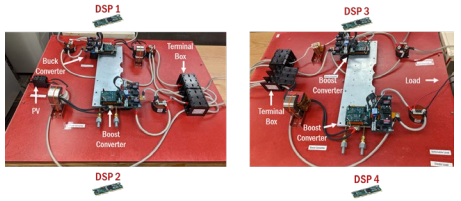
Layer 3: Dc-energy Router based Control

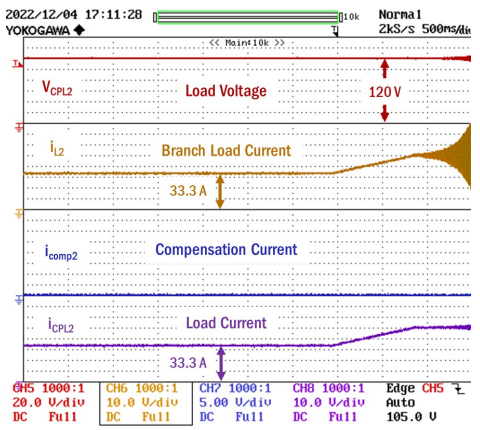
Accomplishments

- Smart Resistor based control for power flow regulation, transient response and stability improvement
- Electronics circuit and battery pack designs for the Dc-energy router
- Hardware test bed design
- Real-time simulation model of interconnected microgrids and the digital twin of the hardware test bed









Ongoing and Planned Work

- Hardware test bed implementation
- Integration of Dc Energy routers and function validations
- Demonstrations

Watts on the Moon - A NASA Challenge for the Near Future

Electric Moon: An OSU Student/Faculty Team

The Challenge

- Transfer 1.5 kW power over 3 km on the moon surface
- The total weight of the power conversion, energy storage and transmission system needs to be lower than 150 kg

Specifications

- Power source voltage: 120 V
- Load voltage: 24-32 V
- Ambient condition: 77 K and 10-3 Torr

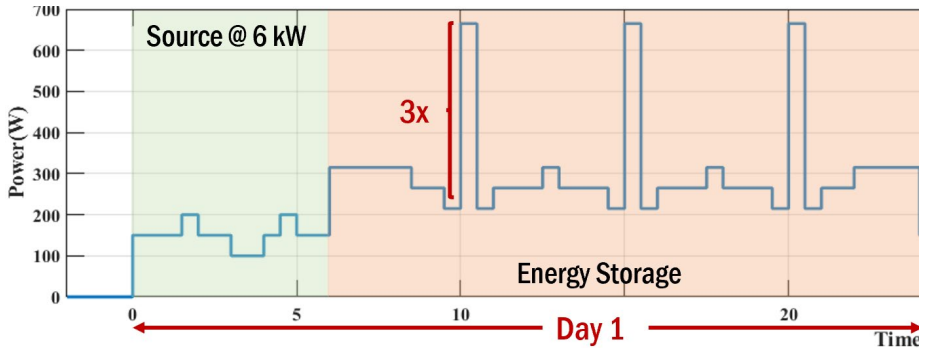
Solution and Approaches by the Electric Moon Team

- 1.5 kV high voltage dc transmission with modular multilevel converter based dc/dc converters
- GaN GIT and Nanocrystalline based converter and transformer designs
- LiFePO4 batteries with multi-layered thermal insulation

Expected Total Weight and Converter Efficiency

- Total weight: 77.61 kg
- Converter efficiency: 97.7%

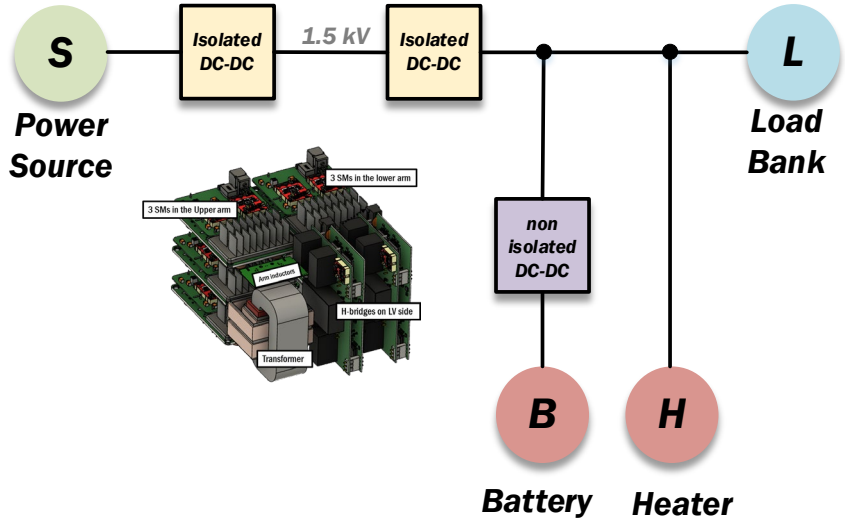
Operation Profile



(2 days, 48 hrs, Day2 identical to Day1)

Grand Prize: $1 M

System Architecture

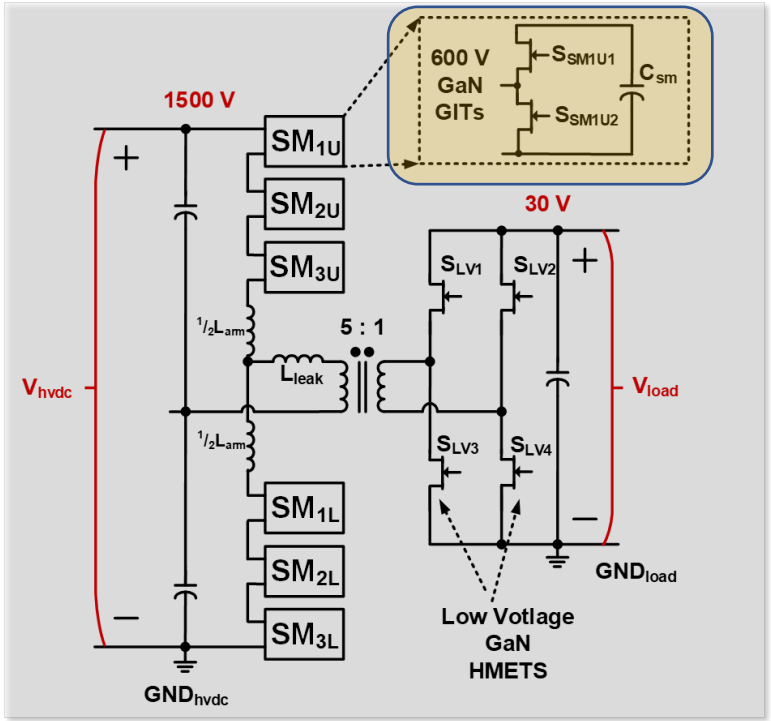


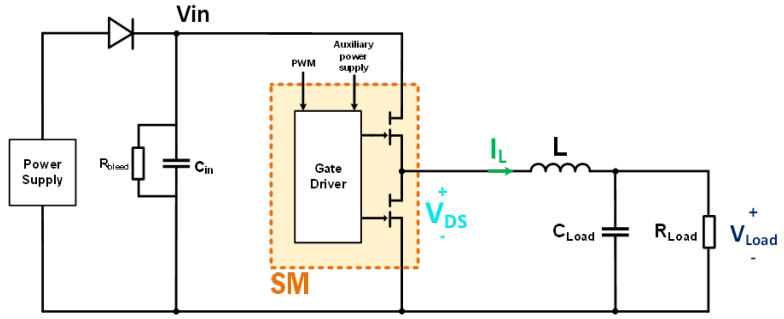
NASA Watts on the Moon Challenge/OSU Electric Moon Team

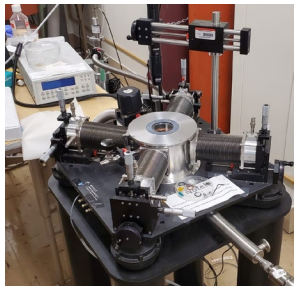
Submodule Demonstration

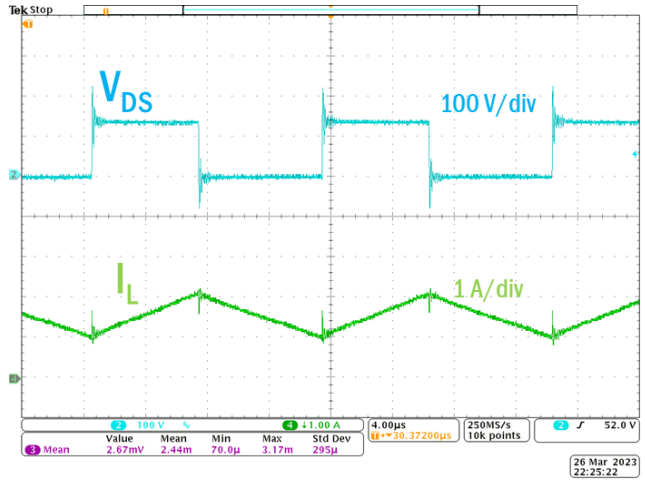
- Testing a submodule (SM) of the isolated dc/dc converter in the vacuum and cryogenic environment.
- The SM is controlled to operate as a buck converter in this demonstration.

	Required conditions in Level 3	Test conditions in the chamber
Temperature	77 K	77 K
Pressure	$< 10^{-3}$ Torr	$< 10^{-6}$ Torr





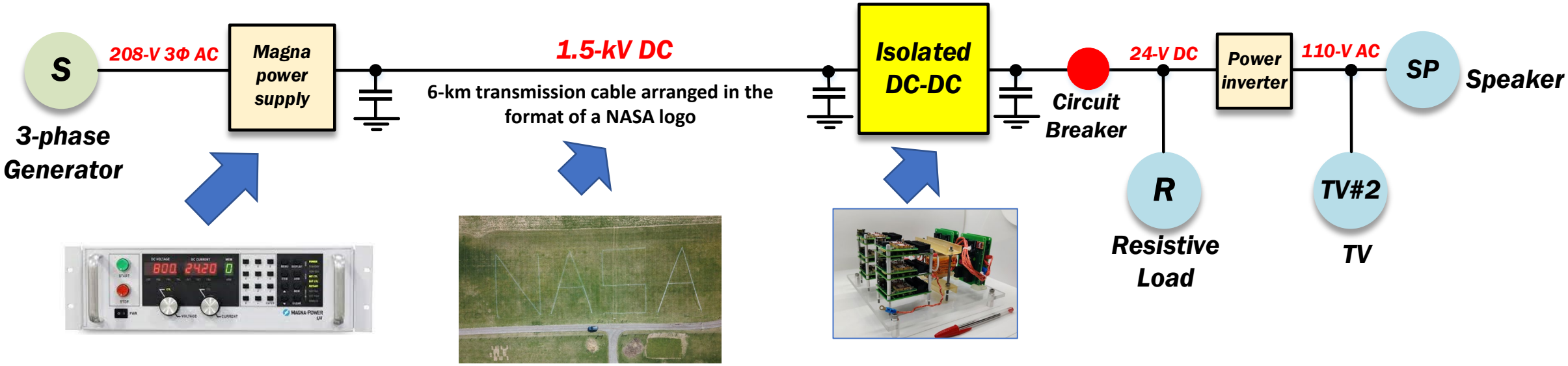




THE OHIO STATE UNIVERSITY

NASA Watts on the Moon Challenge/OSU Electric Moon Team

System Demonstration



- 1.5-kV power distribution enabled by Gallium Nitride (GaN) based multilevel converter
- 3-km transmission with 6-km long cables (AWG 22 3.3 kV rated)
- A combination of loads including resistor loads, TV, speaker, etc.
- Expected efficiency of the isolated dc/dc converter: >98%

Thank you for your attention!

Questions?


APL
JOHNS HOPKINS
APPLIED PHYSICS LABORATORY